

Digital Implementation of Bus Clamped Space Vector Modulation

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Abstract - Space vector modulation has recently become a popular PWM method of supplying a high performance drive. An adaptation of SVM modulation is presented here. This system is called Bus Clamped Space Vector Modulation. This method has some practical advantages when compared to normal SVM. These include a reduced average switching frequency, easy digital implementation and asynchronous control and switching frequencies.

Keywords - PWM, Space Vector Modulation, Bus Clamped

I. INTRODUCTION

Recently *Space Vector Modulation (SVM)* has gained ground as an effective means of generating PWM for vector controlled drives. SVM's success can mainly be attributed to its succinct calculation method and its easy digital implementation. With digital implementations where the control system also calculates the PWM, using programmable counters to output the PWM, SVM can be awkward. A modification of SVM is therefore developed.

With conventional PWM systems all three legs of the inverter are switching continuously. Bus clamped systems clamp one inverter leg to a supply rail while the other are switching. The choice of the clamped

leg depends on the orientation of the desired voltage reference. The remaining two inverter legs are then used to construct the desired voltage. Obviously this has a considerable effect on inverter losses. As should be expected it also increases the harmonic content of the generated wave. This small increase is however compensated for by the greater ease of implementation.

Bus clamped PWM systems are not new. These systems are usually done by fiddling with the reference sine wave used with the normal sawtooth or triangular modulating wave [1]. These implementations suffer from the same shortcomings as normal analogue PWM methods. In this work a new and completely digital implementation of a bus clamped system is presented. This system uses the well-known SVM time equations. It is therefore labelled *Bus Clamped Space Vector Modulation (BCSVM)*.

II. PWM HARDWARE

In order to understand the reasons for the advantages of BCSVM it is first necessary to present the basic hardware on which it is implemented.

The processor used for the control loop calculations are also used for the PWM calculations. Digital counters are used for the PWM output. These counters are shown in Fig. 1. In this figure only the two 8254 counter ICs are shown. The one is used for direct PWM output, and the other is used to generate the frequency of the PWM. There are two timers on U1 that can be used for other system functions. The decoding circuits for software access are not shown.

The 8254 counters can be programmed to be in a required mode. The mode that is used for PWM generation is the Hardware Retriggerable One-shot. In this mode a transition of an OUT from a high to a low logic state occurs after the counter time has elapsed. The G inputs serve as RESET signals.

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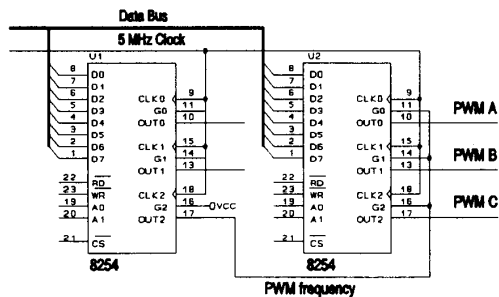


Fig. 1. Digital PWM by programmable counters.

When the **RESET** is received the counter repeats the previous count if no new count has been received, or perform the next count if a new value has been received. All three PWM counters on U2 receive a **RESET** signal on the G inputs from OUT2 on U1 at the same time. This means that there will be a simultaneous change of state for the three PWM channels. This limits these counters in the method of PWM that can be applied.

By placing further programmable logic on the PWM lines, the PWM can be inverted on alternate cycles. If the control program is synchronized with the PWM, the first instruction in the program can be set to invert the PWM signals. If this is done the simultaneous switching point does not occur and the PWM signal can be made to resemble a triangular wave modulation.

III. SPACE VECTOR MODULATION

Because BCSVM is based on SVM principles it is first necessary to consider the generation of SVM before BCSVM can be explained.

SVM ([2] and [3]) is a method of PWM and, as the name implies, it is related to the voltage vector. The essence of SVM is that an inverter has a finite number of switching states. For a three-phase inverter with three legs and two switching elements in each of them, there are eight possible switching combinations (assuming that one switch in a leg is closed and the other open). There are thus eight distinctive voltage vectors available. Two of these eight switching positions result in a zero voltage vector (top three switches closed or bottom three closed). In Fig. 2 the six possible switching positions that result in a non-zero voltage are shown. The principle of SVM is to use these eight switching positions (voltage phasors) to

generate a voltage in any direction with any magnitude lower than the supply limitations.

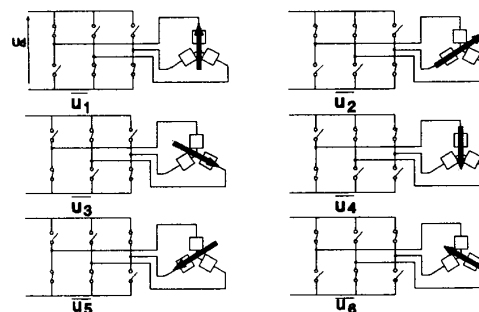


Fig. 2. Inverter switching states with their corresponding voltage vectors.

Fig. 3 shows the basic voltage vectors in a different sequence and phase relationship to that of Fig. 2. The switching vectors in Fig. 3 are symmetrically placed at 60° intervals. The area between any two contiguous vectors is called a sector. The importance of such sectors are that, should the desired voltage vector at any stage fall in a particular sector, then only the flanking switching voltage vectors and zero voltage vectors are used to construct the desired voltage phasor. Because of the symmetry of the switching vectors and sectors, it is only necessary to explain the operation in one of these sectors in order to formulate the equations governing SVM.

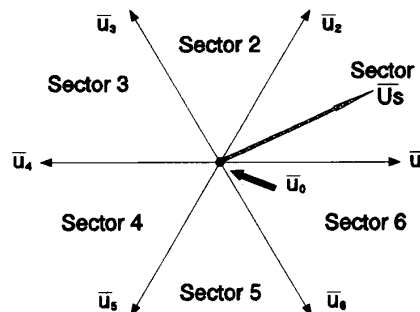


Fig. 3. Switching vectors and the desired vector.

A generalized sector is shown in Fig. 4. \bar{u}_s is the desired voltage vector at that instant. \bar{u}_a and \bar{u}_b are any two adjacent vectors from Fig. 3. During one sampling interval, Δt , both \bar{u}_a and \bar{u}_b and one of the zero voltage vectors must be selected. Another requirement is that the switching frequency should be constant. This ensures that the silicon switches can operate at their maximum frequency. To ensure this, each inverter switch must only be used once during

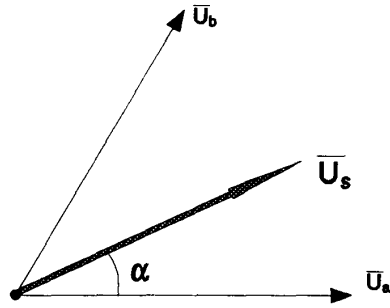


Fig. 4. A typical position of the desired vector in a general sector.

each cycle. The only way to accomplish this is to make use of a forward and a reverse cycle. During the forward cycle in an uneven sector number, all the legs of the inverter switch to the positive rail. In a reverse cycle the switching takes place to the negative rail. A sequence of a forward and reverse cycle is called a switching set. If the sector number has changed between cycles, the first cycle in the new sector must begin in an opposite direction to the last cycle in the previous sector. A switching set in the generalized uneven sector is shown in Fig. 5.

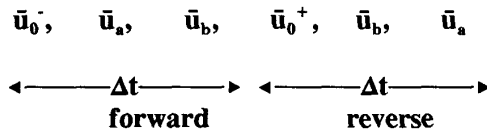


Fig. 5. Switching set in a general odd numbered sector.

The switching frequency of the inverter is defined as the frequency of repetition of switching sets, $1/(2\Delta t)$. The device, hardware or software, controlling the inverter can therefore get two voltage command signals into a single inverter switching cycle. This means that the control frequency can be double that of the inverter's switching frequency. It can be very useful when the dynamics of the system demand a faster control sampling frequency than the inverter is capable of. This is similar to the result obtained with digital triangular modulation.

The process is now straightforward in that it is only necessary to calculate the portions of sampling period allocated to \bar{u}_a , \bar{u}_b and \bar{u}_0 . The time weighted sum of these vectors taken over the sampling period, Δt , should give the desired voltage vector \bar{u}_s . [3] and [4], in a slightly different format, provide the

solution to this time weighing as:

$$t_a = \frac{9}{\pi^2} |\bar{u}_s| \Delta t \left(\cos \alpha - \frac{1}{\sqrt{3}} \sin \alpha \right) \tag{1}$$

$$t_b = \frac{6\sqrt{3}}{\pi^2} |\bar{u}_s| \Delta t \sin \alpha \tag{2}$$

$$t_0 = \Delta t - t_a - t_b \tag{3}$$

where: $|\bar{u}_s|$ is \bar{u}_s normalised to base of $6u_d/\pi^2$, u_d is the dc link voltage and α is the angle between the desired vector, \bar{u}_s , and the switching vector, \bar{u}_a , in the generalized sector.

This definition of SVM is still not complete. If a too high $|\bar{u}_s|$ is used in these equations the time allocated to t_a plus t_b will be longer than Δt . It is therefore necessary to only allow normalised \bar{u}_s voltages less than 0.949 in these equations.

Fig. 6 shows the switching of the inverter legs in sectors one and two. With the signal in the low position the lower switch of the corresponding inverter leg is closed.

		FORWARD			REVERSE		
Sector 1	A	t_0	t_a	t_b	t_0	t_b	t_a
	B	\bar{u}_0	\bar{u}_1	\bar{u}_2	\bar{u}_0	\bar{u}_2	\bar{u}_1
	C						
Sector 2	A	t_0	t_b	t_a	t_0	t_a	t_b
	B	\bar{u}_0	\bar{u}_3	\bar{u}_2	\bar{u}_0	\bar{u}_2	\bar{u}_3
	C						

Fig. 6. Switching sequence.

IV. BUS CLAMPED SPACE VECTOR MODULATION

When the SVM equations are used but only the forward or the reverse cycle is used, BCSVM is obtained. Bus Clamped SVM is labelled thus, because each of the legs of the inverter is alternately (depending on the sector) clamped to the dc bus. In the switching sequences for SVM shown in Fig. 6 it can be seen that while the voltage vector \bar{u}_s stays in a single sector, and only a forward or reverse cycle is used, one of the phase legs stays in one position. It is clear that this constitutes a 33% reduction in the

average switching frequency. This reduced average switching frequency is defined as the effective switching frequency. It must however be remembered that this reduction is only an average reduction during half a rotation of the reference vector \bar{u}_s .

If the output frequency is low, the effective switching frequency and output current can not be raised to the rating of the switching elements because heating fluctuations at double the output frequency will occur. The switching elements may then overheat during a part of each output half cycle. At higher output frequencies these fluctuations will be damped by the thermal inertia of the semiconductors. With this reduced average inverter switching frequency, [1]'s labelling of BCSVM as "Inverter loss optimised space vector PWM" can be understood.

V. EVALUATION OF BCSVM

BCSVM considerably decreases the complexity of allowing the inverter to switch at a higher frequency than the control loop frequency (asynchronous switching). This is because the digital counters used retain the previous cycle's duty cycle. If a new duty cycle is not written to the counters, the old duty cycle is repeated. Therefore, if the inverter is to operate at a switching (not effective) frequency of 8 kHz, and the control loop is operated at 2 kHz, the same average reference voltage will be produced by the PWM for 4 switching cycles. This is extremely beneficial for the operation of a vector control drive when faster control frequencies cannot be obtained with the available computing power, but a faster inverter is available or required. For example, the frequency rating of the cheap semiconductors used for small inverters is often much higher than the control frequency that can be achieved with cheap digital control. In such cases BCSVM will be very useful.

Another major advantage of BCSVM is that (as with SVM) there is an increase of 15 % in the maximum line-to-line voltage obtainable, without overmodulation, with a given dc link voltage when compared to triangular sinusoidal modulation. Sinusoidal modulation is able to produce a peak line-to-line voltage of 87 % of the dc link, [5]. This effectively means that BCSVM is able to return the full ac voltage from which the dc link was rectified (large smoothing capacitor assumed). This together with the vector nature of BCSVM makes it extremely suitable for vector control applications.

The programmable counters allow for the unsynchronised updating of the counter's duty cycles.

It is therefore possible for the PWM frequency to be higher than the control frequency. E.g., a control frequency of 2 kHz is sufficient for most digital motor control systems. In this case the control system generates a new voltage command every 0.5 ms. FET and IGBT inverters are capable of much higher switching frequencies. With BCSVM and the programmable timers it is possible to repeat this voltage signal automatically for a number of cycles. BCSVM therefore allows the full utilization of the inverter's switching frequency capability.

In Fig. 7 the measured control signal of one inverter leg is shown. This signal was measured at logic level and not at the inverter's terminals. The 33 % non-switching portion of the leg is clearly visible. Fig. 8 displays an expanded portion of this signal.

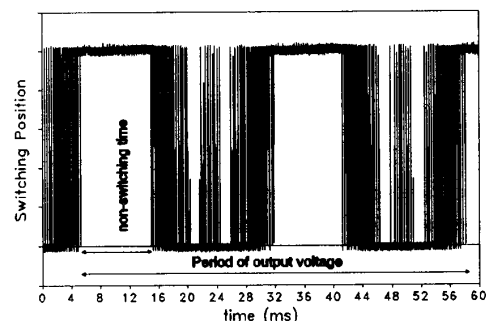


Fig. 7. Output voltage of one leg using BCSVM.

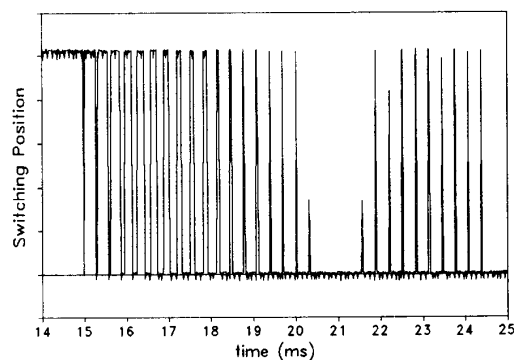


Fig. 8. Fig. 7 on an expanded time scale.

VI. CONCLUSIONS

There are numerous analogue implementations of bus clamped systems ([5] and [6]). These systems use modified sine waves that are modulated to obtain the

PWM. These methods suffer from the same limitations as analogue PWM. Digital implementations of these methods are cumbersome to implement.

A completely digital implementation of a bus clamped PWM system is presented. This system uses the SVM equations to calculate the switching times. The use of programmable timers for the output of the PWM allows it to utilize the control processor for PWM calculation. The PWM frequency may also be higher than the control frequency. Asynchronous operation of the control and PWM is also possible due to the memory register of the programmable counter.

This PWM system has been tested with very good results on a rotor flux vector controlled induction motor, and produced excellent results. This control system was implemented on a single transputer system. A control frequency of 2 kHz was used while the inverter switched at 6 kHz with the use of this PWM system.

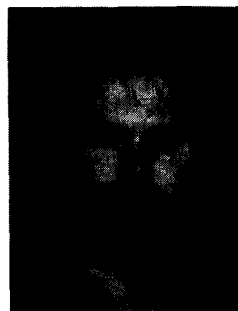
VII. ACKNOWLEDGEMENTS

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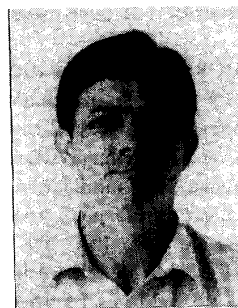
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